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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No. 0819-261

First Inventor or Application Identifier: Masaaki NISHIJIMA

Title: SEMICONDUCTOR DEVICE

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [ ] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [39]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [12]
4. [ ] Oath or Declaration *Total Pages* [ ]
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ADDRESS TO:

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6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
   (when there is an assignee)
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement [X] Copies of IDS Citations
    (IDS)/PTO-1449
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. [ ] *Small Entity [ ] Statement filed in prior application, Status still proper and desired
    Statement(s) (PTO/SB/09-12)
15. [X] Certified Copy of Japanese Priority Document
    No. 10-198269 Filed: July 14, 1998
16. [ ] Other:

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
    [ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No. _____
    Prior application information: Examiner:_____ Group/Art Unit:_____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re NEW PATENT Application of	)
Masaaki NISHIJIMA	)
Serial No. Not Yet Assigned	) Attn: Applications
Filed: July 12, 1999	) Branch
For: SEMICONDUCTOR DEVICE	) Date: July 12, 1999

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

Page 15, after line 25, insert the following description:

--Figures 17A and 17B are cross sectional views of alternative line structures for a semiconductor device according to a first embodiment of the present invention.

Figure 18 is a cross-sectional view of a line structure for a semiconductor device according to a fourth embodiment of the present

invention.--.

REMARKS

The specification has been amended to include the descriptions of Figures 17 and 18 to the subject application.

Examination on the merits is requested.

Respectfully submitted,

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SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention generally relates to a microwave integrated circuit, and more particularly relates to a microstrip line structure for a semiconductor device operable at radio frequencies, which contributes to downsizing and performance enhancement of mobile communications unit terminals.

In recent years, the applications of mobile communications terminals of various types, including cellular phones and portable communications terminals, have been spanning a wider and wider range over the world. In Japan, cellular phones, operating on 900 MHz and 1.5 GHz bands, and personal handy phone systems (PHS), operating on 1.9 GHz band, have been popularized. Globally speaking, European GSM and DECT phones and American PCS phones are very popular.

Among these numerous types of mobile communications unit terminals, portable communications terminals, in particular, are required to be as small in size and as light in weight as possible. Thus, first of all, components for a portable communications terminal should have its size reduced and its performance enhanced. For example, to downsize a power amplifier for use in a radio-frequency transmitter for a portable communications terminal (hereinafter, simply referred to as an "RF power amplifier"), it is strongly needed to imple-

ment the RF power amplifier as a monolithic microwave IC (MMIC) of GaAs. In an MMIC, active components, matching circuit and bias supply are all integrated on a single chip. Thus, an MMIC can more effectively contribute to downsizing than a hybrid IC (HIC), in which matching circuit and bias supply are implemented as discrete chip components.

From a viewpoint of performance enhancement, however, an MMIC is said to be inferior to an HIC. This is because if an RF power amplifier is implemented as an MMIC, for instance, then parasitic resistive components, such as interconnection resistance, which are involved with semiconductor device processing for fabricating the MMIC, adversely increase, thus causing a considerable loss of the power to be transmitted. For that reason, a power amplifier implemented as an MMIC often results in lower power gain, lower power amplification and deteriorated distortion characteristic compared to a power amplifier implemented as an HIC. Thus, according to the currently available techniques, it is determined based on a necessary trade-off between downsizing and performance enhancement which part of a power amplifier should be implemented as an MMIC.

Hereinafter, an exemplary MMIC implementation of output matching circuit and drain-biasing circuit will be described with reference to Figures **10** through **15**. An exemplary microstrip line structure will also be described with reference to

Figure **16.** A microstrip line structure is a basic structure of a spiral inductor used as a passive component in the output matching circuit and drain-biasing circuit.

Figure **10** illustrates a planar pattern for a final-stage MESFET and an output matching circuit thereof used for a high-output power amplifier transmitting a power of about 1 W. Following is respective parameters of the final-stage MESFET.

Unit finger length: 300μm

Total gate width: 24 mm

Frequency: 900 MHz

Power supply voltage: 3.5 V

Saturated output power with idle current of 400 mA supplied: about 1.5 W

Operating current: about 550 mA

Gain: about 12 dB

The gate of the MESFET **410** is connected to a gate-biasing pad **412** via a gate electrode extended line **411.** The source of the MESFET **410** is connected to an MIM capacitor **409** via a source pad **413.** The drain of the MESFET **410** is connected to a drain-biasing pad **415** via a drain extended line **414.** One terminal of a spiral inductor **408** is connected to a part of the drain extended line **414,** while the other terminal thereof is connected to an output pad **416** via the MIM capacitor **409.**

The line of the spiral inductor **408** is made of gold plated to be about 3 μm thick. The extended lines thereof are formed by evaporating and depositing titanium and gold thereon. The upper-layer conductor of the MIM capacitor **409** is made of gold plated, while the lower-layer conductor thereof is formed by evaporating and depositing titanium and gold thereon. The interlayer dielectric film of the capacitor **409** is formed by depositing silicon nitride (SiN_x) with a dielectric constant of about 7 by a CVD process.

In the MMIC including the output matching circuit, the final-stage MESFET operates at a frequency of 900 MHz with a current of about 560 mA supplied. The MESFET provides a saturated output power of about 1.0 W with a power supply voltage of 3.5 V applied, and shows a gain of about 10 dB.

Figure **11** illustrates an equivalent circuit of the MESFET and output matching circuit thereof shown in Figure **10**. A MESFET shown in Figure **11**, including gate **302**, source **303** and drain terminals **304**, corresponds to the MESFET **410** shown in Figure **10**. Equivalent series inductor **305**, equivalent series resistor **306** and equivalent parallel capacitor **307** are connected to the drain terminal **304** of the MESFET. The equivalent series indictor **305** and resistor **306** form an equivalent circuit of the spiral inductor **408**. In this example, the inductance value of the equivalent series inductor **305** is about 2.5 nH, the resistance value of the equivalent

series resistor **306** is about 4Ω and the capacitance value of the equivalent parallel capacitor **307** is about 12 pF. The equivalent parallel capacitor **307** corresponds to the MIM capacitor **409** shown in Figure **10**.

Figure **12** illustrates a location of load impedance Z_L **301** of the MESFET on a Smith chart showing impedance matching from a 50Ω line. The load impedance Z_L **301** can be impedance-matched with the center of the Smith chart at 50Ω by tracing paths formed by the parallel capacitive components and series inductive components. In this case, the value of the load impedance Z_L **301** is 7Ω+j4Ω.

Next, a drain-biasing circuit and a MESFET, in which a drain choking inductor is implemented as a part of an MMIC, will be described with reference to Figure **13**. The choking inductor is a device used for preventing radio frequency power from leaking to the drain power supply.

Following is respective parameters of the MESFET.

Unit finger length: 100μm

Total gate width: 1 mm

Frequency: 900 MHz

Power supply voltage: 3.5 V

Saturated output power with idle current of 20 mA supplied: about 120 mW

Operating current: about 23 mA

Gain: about 13 dB

The gate of the MESFET **505** is connected to a gate-biasing pad **507** via a gate electrode extended line **506**. The source of the MESFET **505** is connected to a source pad **508**. The drain of the MESFET **505** is connected to a drain extended line **509**. Part of the drain extended line **509** is connected to a drain-biasing pad **510** via a spiral inductor **504**.

In the MMIC including the drain choking inductor, the MESFET operates at a frequency of 900 MHz and with a power supply voltage of 3.5 V applied and a current of about 19 mA supplied. The MESFET provides a saturated output power of about 90 mW with an idle current of 20 mA supplied, and shows a gain of about 11 dB.

The line of the spiral inductor **504** is made of gold plated to be about 3 μm thick. The extended lines thereof are formed by evaporating and depositing titanium and gold thereon.

Figure **14** illustrates an equivalent circuit of the MESFET **505** and the drain-biasing circuit shown in Figure **13**. An equivalent series inductor **502** and an equivalent series resistor **503** constitute an equivalent circuit of the spiral inductor **504** shown in Figure **13**. In this example, the inductance value of the equivalent series inductor **L 502** is 21 nH and the resistance value of the equivalent series resistor **R 503** is 7.5Ω.

Figure **15** illustrates the location of choke impedance Z_c

501 on a Smith chart. The choke impedance is located at a drain terminal of the MESFET, which is short-circuited at an end through which a drain voltage is applied. Usually, the choke impedance Z_c **501** is ideally defined to be open. But since the choke impedance is sometimes used as a matching circuit in practice, the choke impedance is not necessarily open. In the example shown in Figure **15**, the choke impedance Z_c **501** is located at an angle of phase rotation of about 140 degrees.

Figure **16** illustrates the cross section of a microstrip line structure, which is a basic structure of a spiral inductor. As described above, a spiral inductor is used as a passive component for an output matching circuit or a drain-biasing circuit. Such a line structure includes: a line **602** formed on the surface of a GaAs substrate **601**; and a grounded conductor **603** formed on the back of the GaAs substrate **601**. The line **602** may be made of gold plated to be about 3 μm thick, for example.

In the first prior art example illustrated in Figures **10** through **12**, the output impedance of the final-stage GaAs FET used as a power amplifier is as low as about 10 Ω or less. Accordingly, the resistive components of the output matching circuit, including the interconnection resistance of the spiral inductor formed on the GaAs substrate, increases the power lost by the output matching circuit. As a result, the power

amplifier shows lower gain, lower power amplification (corresponding to operating current) and deteriorated distortion characteristic. In order to avoid problems such as these, the thickness or width of a line may be increased. However, the thickness of a line cannot exceed a certain upper limit defined by various restrictions on semiconductor device processing. Also, the wider a line, the larger the area occupied by the line on a chip, which is contradictory to the demand of downsizing.

Even in a medium-output power amplifier transmitting a power of about 100 W, the input, interstage and output matching circuits thereof are included in an MMIC. In such a case, the output matching circuit is built in an MMIC, in which the output impedance of a final-stage GaAs FET used for the power amplifier is as high as approximately 300 Ω or more. Even so, the resistive components of the output matching circuit, including the interconnection resistance of the spiral inductor formed on the GaAs substrate, increases the power lost by the output matching circuit, thus adversely affecting the performance thereof.

In the second prior art example shown in Figures **13** through **15**, since the drain-biasing circuit is implemented as a part of an MMIC, the choking spiral inductor occupies a larger area on a GaAs substrate, thus increasing the area of the MMIC chip and interfering with downsizing. Furthermore, a

drain voltage externally applied drops due to the parasitic resistance of the spiral inductor line, resulting in deterioration in performance of the power amplifier. Accordingly, the second prior art example cannot make full use of the essential characteristics of the power amplifier, and cannot sufficiently contribute to the performance enhancement thereof.

SUMMARY OF THE INVENTION

An object of the present invention is providing a semiconductor device operable at radio frequencies, which can contribute to both downsizing and performance enhancement of mobile communications terminals.

A semiconductor device according to the present invention has a line structure formed on a semiconductor substrate. The line structure includes: a conductor layer formed on the semiconductor substrate; a dielectric film formed on the conductor layer; and a conductor line formed on the dielectric film. The dielectric film includes: a first dielectric portion, at least part of the first dielectric portion being located between the lower surface of the conductor line and the upper surface of the conductor layer; and second and third dielectric portions laterally arranged to interpose the first dielectric portion therebetween. The dielectric constant of the first dielectric portion is different from at least one of the dielectric constants of the second and third dielectric

portions.

In one embodiment of the present invention, the dielectric constant of the first dielectric portion may be lower than those of the second and third dielectric portions.

In another embodiment of the present invention, at least one of the dielectric constants of the second and third dielectric portions may be higher than 10.

In still another embodiment, the device may further include another dielectric film covering the conductor line.

Another semiconductor device according to the present invention also has a line structure formed on a semiconductor substrate. The line structure includes: a conductor layer formed on the semiconductor substrate; a dielectric film formed on the conductor layer; and a conductor line formed on the dielectric film. The dielectric film includes two or more dielectric layers with mutually different dielectric constants.

In one embodiment of the present invention, at least one of the two or more dielectric layers may include: a first dielectric portion, at least part of the first dielectric portion being located between the lower surface of the conductor line and the upper surface of the conductor layer; and second and third dielectric portions laterally arranged to interpose the first dielectric portion therebetween. The dielectric constant of the first dielectric portion may be different from at

least one of the dielectric constants of the second and third dielectric portions.

In another embodiment of the present invention, at least one of the two or more dielectric layers has preferably been patterned.

Still another semiconductor device according to the present invention also has a line structure formed on a semiconductor substrate. The line structure includes: a conductor layer formed on the semiconductor substrate; a first dielectric film formed on the conductor layer; a conductor line formed on the first dielectric film; and a second dielectric film covering the conductor line.

In one embodiment of the present invention, the first dielectric film may include two or more dielectric layers with mutually different dielectric constants.

Yet another semiconductor device according to the present invention also has a line structure formed on a semiconductor substrate. The line structure includes: a conductor layer formed on the semiconductor substrate; a dielectric film formed on the conductor layer; and a conductor line formed on the dielectric film. A region of the conductor layer, which is located under the conductor line, has been removed at least partially.

In one embodiment of the present invention, the dielectric film may include two or more dielectric layers with mu-

tually different dielectric constants.

In another embodiment of the present invention, the device may further include a second dielectric film covering the conductor line.

In still another embodiment, the dielectric constant of the second dielectric film may be higher than 10.

Yet another semiconductor device according to the present invention also has a line structure formed on a semiconductor substrate. The line structure includes: a coplanar conductor layer formed over the semiconductor substrate; and a dielectric film formed on the coplanar conductor layer. The coplanar conductor layer includes: a grounded conductor layer; and a conductor line spaced apart from the grounded conductor layer. The dielectric constant of the dielectric film is higher than 10.

In one embodiment of the present invention, a dielectric with a dielectric constant equal to or smaller than 10 may exist between the grounded conductor layer and the conductor line.

Yet another semiconductor device according to the present invention also has a line structure formed on a semiconductor substrate. The line structure includes: a first dielectric film formed on the semiconductor substrate; a coplanar conductor layer formed on the first dielectric film; and a second dielectric film formed on the coplanar conductor

layer.

In one embodiment of the present invention, the dielectric constant of at least one of the first and second dielectric films may be higher than 10.

In another embodiment of the present invention, the first dielectric film may include two or more dielectric layers with mutually different dielectric constants.

In still another embodiment, the device may further include an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

According to the present invention, the equivalent dielectric constant of a dielectric film can be optimized. In addition, the line length of a spiral inductor, which is required for matching the impedance of an active component with a desired load impedance or attaining a desired choke inductance, can be shortened, thus reducing the parasitic resistive components involved with the spiral inductor. As a result, it is possible to provide a semiconductor device operable at radio frequencies and contributing to both downsizing and performance enhancement of mobile communications unit terminals.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure **1** is a cross-sectional view of a line structure

for a semiconductor device according to a first embodiment of the present invention.

Figures **2A**, **2B**, **2C**, **2D**, **2E** and **2F** are cross-sectional views illustrating respective process steps for forming the line structure of the first embodiment.

Figures **3A** illustrates an equivalent circuit of the line structure of the first embodiment; and

Figure **3B** is a Smith chart illustrating respective angles of phase rotation for a microstrip line with the structure shown in Figure **1** and a conventional line structure shown in Figure **16**.

Figure **4** is a cross-sectional view of a line structure for a semiconductor device according to a second embodiment of the present invention.

Figures **5A**, **5B**, **5C** and **5D** are cross-sectional views illustrating respective process steps for forming the line structure of the second embodiment.

Figure **6** is a Smith chart illustrating respective angles of phase rotation for a microstrip line with the structure shown in Figure **4** and the conventional line structure shown in Figure **16**.

Figure **7** is a cross-sectional view of a line structure for a semiconductor device according to a third embodiment of the present invention.

Figures **8A**, **8B** and **8C** are cross-sectional views illus-

trating respective process steps for forming the line structure of the third embodiment.

Figure **9** is a Smith chart illustrating respective angles of phase rotation for a microstrip line with the structure shown in Figure **7** and the conventional line structure shown in Figure **16**.

Figure **10** is a plan view illustrating a final-stage MESFET and an output matching circuit thereof used for a high-output power amplifier transmitting a power of about 1 W.

Figure **11** is an equivalent circuit diagram of the MESFET and output matching circuit thereof shown in Figure **10**.

Figure **12** is a Smith chart illustrating a location of load impedance Z_L **301** of the MESFET shown in Figure **11** and showing impedance matching from a 50Ω line.

Figure **13** is a plan view illustrating a MESFET and a drain-biasing circuit thereof.

Figure **14** is an equivalent circuit diagram of the MESFET and drain-biasing circuit thereof shown in Figure **13**.

Figure **15** is a Smith chart illustrating the location of choke impedance Z_c **501** at a drain terminal of the MESFET, which is short-circuited at an end through which a drain voltage is applied.

Figure **16** is a cross-sectional view illustrating a microstrip line structure, which is a basic structure of a conventional spiral inductor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, preferred embodiments of a semiconductor device according to the present invention will be described with reference to the accompanying drawings.

EMBODIMENT 1

A first exemplary embodiment of a semiconductor device according to the present invention will be described with reference to Figures **1** through **3**.

Figure **1** illustrates the cross section of a novel microstrip line structure or a waveguide applicable to the semiconductor device of the present invention. As shown in Figure **1**, this line structure includes: a grounded conductor layer **102** made up of plural pairs of titanium and gold layers alternately stacked to be about 0.7μm thick on the surface of a GaAs substrate **101**; and a gold-plated line (conductor line) **105** provided over the grounded conductor layer **102** to be spaced apart therefrom. A dielectric film (thickness: about 0.1 μ m to about 2 μ m) is formed on the grounded conductor layer **102**. The dielectric film includes: a strontium titanate ($SrTiO_3$ or STO) layer **103**; and a dielectric **104** of silicon nitride (SiN_x). In this embodiment, the SiN_x dielectric **104** is approximately as thick as the strontium titanate layer **103**, is in contact with the lower surface of the line **105** and is located in a region between the lower surface of the line **105**

and the upper surface of the grounded conductor layer **102**. In other words, the SiN_x dielectric **104** is laterally sandwiched by the strontium titanate layer **103**. The dielectric constant of the SiN_x dielectric **104** is in the range from about 6 to about 7, which is much lower than that of the strontium titanate layer **103** in the range from about 50 to about 200.

An active component operable at radio frequencies (hereinafter, simply referred to as an "RF active component"), like a MESFET as described in the background section, is actually formed on the GaAs substrate **101**, but is not shown in Figure **1** for the sake of simplicity. The line structure shown in Figure **1** is used for forming the spiral inductor shown in Figure **10** or **13**, and is electrically connected to the RF active component and so on.

Hereinafter, a method for forming the line structure will be described with reference to Figures **2A** through **2F**.

First, as shown in Figure **2A**, the grounded conductor layer **102**, made up of titanium and gold layers alternately stacked, is deposited on the GaAs substrate **101** by a thin film deposition technique like evaporation. The thickness of the grounded conductor layer **102** is defined within the range from 0.5μm to 3μm. The grounded conductor layer **102** is not necessarily made of titanium and gold, but may be made of platinum (Pt) and tungsten silicon nitride (WSiN).

Next, as shown in Figure **2B**, the strontium titanate

layer **103** with a dielectric constant of about 100 is deposited by RF sputtering to be about 1.5 μm thick on the grounded conductor layer **102**. Thereafter, a resist **106** is applied onto the strontium titanate layer **103**, and then exposed to radiation and developed by a photolithographic process, thereby providing an opening **107** in the resist **106**. The width **108** of the opening **107** may be about 10 μm. The planar layout of the opening **107** is defined so as to correspond to that of the line **105** to be formed during a subsequent process step.

Then, as shown in Figure **2C**, portion of the strontium titanate layer **103**, which is exposed inside the opening **107**, is etched away by an ion milling technique, for example, to form a recess (opening) **109** in the strontium titanate layer **103**. The width of the recess **109** is substantially equal to the width **108** of the opening **107**. This etching process is performed so as to expose the surface of the grounded conductor layer **102** at the bottom of the recess **109**.

Subsequently, as shown in Figure **2D**, a silicon nitride portion (SiN_x dielectric) **104** (with a dielectric constant of about 7 in this embodiment) is formed to be about 1.5 μm thick within the recess **109** of the strontium titanate layer **103** by a thin film deposition technique such as a plasma CVD process. The silicon nitride portion **104** may be formed by a lift-off technique, for example.

Thereafter, as shown in Figure **2E**, the gold-plated line

105 is formed on the dielectric **104**. In this embodiment, the thickness of the line **105** is 3 μm, the width **110** thereof is 15 μm, and the centerline of the SiN_x dielectric **104** is substantially aligned with that of the line **105**. It should be noted that the centerline of the SiN_x dielectric **104** does not have to be aligned with that of the line **105**. That is to say, the line **105** may partially overlap with the SiN_x dielectric **104** in the planar layout. In such a case, since the equivalent dielectric constant of the dielectric film is set at an appropriate level, the length of the line required for realizing desired impedance matching can be considerably shortened.

Figure **3A** illustrates an equivalent circuit diagram where a spiral inductor such as that shown in Figure **13** is formed to have the line structure just described. Figure **3B** illustrates respective angles of phase rotation for a microstrip line with the structure just described and for the conventional microstrip line structure shown in Figure **16** (hereinafter, simply referred to as a "conventional structure"). In the example illustrated in Figure **3B**, the lengths of these two types of lines are supposed to be equal to each other. Each of these angles of phase rotation represents a phase angle of an associated line on a Smith chart, where the far end of the line is short-circuited. And each angle can be used as an index for estimating a length of a line required

for attaining desired impedance matching. More specifically, the larger the angle of phase rotation of a line, the shorter that portion of the line required for realizing desired impedance matching. As can be seen from Figure **3B**, the angle of phase rotation of the line structure according to this embodiment is about 68 degrees larger than that of the conventional structure of the same length. Thus, according to the present invention, the required line length can be shortened compared to the conventional structure. This is because the equivalent dielectric constant of the dielectric film can be optimized by making up the dielectric film of plural parts with mutually different dielectric constants.

Such effects are attained because a capacitance formed between the grounded conductor layer **102** and the conductor line **105** is reduced and because the electrical length does not increase according to the present invention. The capacitance can be reduced by providing a first dielectric portion made of a material with a lower dielectric constant between the grounded conductor layer **102** and conductor line **105**. On the other hand, the increase in electrical length can be suppressed by interposing the first dielectric portion between a pair of other dielectric portions with higher dielectric constants. Also, the reduction in capacitance contributes to increasing the characteristic impedance Z_0, thus shortening the required line length.

By using such a line structure, the line length of a spiral inductor required for matching the impedance of an active component with a desired load impedance or attaining a desired choke inductance can be shortened, thus reducing the parasitic resistive components involved with the spiral inductor. As a result, it is possible to provide a semiconductor device operable at radio frequencies and contributing to both downsizing and performance enhancement of mobile communications unit terminals.

It should be noted that if another strontium titanate film **111** is deposited to cover the strontium titanate layer **103** and the line **105** as shown in Figure **2F**, then the angle of phase rotation can be further increased. This is because the electrical length can be further shortened by covering the line with a dielectric film having a high dielectric constant.

At least half of the strontium titanate layer **103**, sandwiching the SiN_x dielectric **104** on right- and left-hand sides, preferably has a dielectric constant higher than 10. This is because the electrical length can be drastically reduced by setting the dielectric constant of that portion at 10 or more. Examples of such films with high dielectric constants include a barium strontium titanate (BST) film, as well as a strontium titanate film.

Also, the dielectric film may have a multilayer structure including a first dielectric layer and a second dielec-

tric layer formed on the first dielectric layer. In such a case, the dielectric constant of the first dielectric layer may be either higher or lower than that of the second dielectric layer. By employing this multilayer structure, the equivalent dielectric constant of the dielectric film can be controlled at an appropriate value. Furthermore, after an opening has been provided only in the second dielectric layer, the opening may be filled in with a dielectric having a dielectric constant different from that of the second dielectric layer, and a line may be formed to overlap with the buried dielectric. For example, an opening may be formed only in a second dielectric layer of strontium titanate and then filled in with silicon nitride. In such a case, the equivalent dielectric constant of the dielectric film can be controlled at a desired level even more easily.

Figures **17A** and **17B** illustrate modified examples of this embodiment.

Like the structure shown in Figure **1**, the structure shown in Figure **17A** also includes: the grounded conductor layer **102** made up of plural pairs of titanium and gold layers alternately stacked to be about 0.7μm thick on the surface of the GaAs substrate **101**; and the gold-plated line (conductor line) **105** provided over the grounded conductor layer **102** to be spaced apart therefrom. The structure shown in Figure **17A** further includes: a patterned silicon nitride (SiN_x) portion

104 formed on the grounded conductor layer **102**; and a strontium titanate ($SrTiO_3$ or STO) layer **103** covering the SiN_x portion **104**.

In this modified example, the patterned silicon nitride (SiN_x) portion **104** is formed first, and then the strontium titanate ($SrTiO_3$ or STO) layer **103** is deposited over the substrate **101**.

In the example shown in Figure **17B**, the patterned silicon nitride (SiN_x) portion **104** is formed on the grounded conductor layer **102**, and then the strontium titanate ($SrTiO_3$ or STO) layer **103** is deposited over the substrate **101** to cover the SiN_x portion **104** as in the structure shown in Figure **17A**. However, in the example shown in Figure **17B**, the strontium titanate ($SrTiO_3$ or STO) layer **103** has its upper surface planarized after having been deposited over the substrate **101**.

According to these modified examples, the line length of the spiral inductor or the like can also be shortened as in the embodiment shown in Figure **1**. As a result, the parasitic resistive components can also be reduced.

EMBODIMENT 2

A second exemplary embodiment of a semiconductor device according to the present invention will be described with reference to Figures **4** through **6**.

Figure **4** illustrates the cross section of a novel line

structure applicable to the semiconductor device of the present invention. As shown in Figure **4**, this line structure includes: a grounded conductor layer **202** made up of plural pairs of titanium and gold layers alternately stacked to be about 0.7μm thick on the surface of a GaAs substrate **201**; and a gold-plated line **204** provided over the grounded conductor layer **202** to be spaced apart therefrom. A strontium titanate layer (thickness: about 0.1μm to about 2μm) **203** is formed on the grounded conductor layer **202**. A portion of the grounded conductor layer **202** just under the line **204** has been removed, which is totally different from the line structure of the first embodiment. An RF active component, like a MESFET as described in the background section, is actually formed on the GaAs substrate **101**, but is not shown in Figure **4** for the sake of simplicity.

Hereinafter, a method for forming the line structure will be described with reference to Figures **5A** through **5D**.

First, as shown in Figure **5A**, the grounded conductor layer **202**, made up of titanium and gold layers alternately stacked, is deposited on the GaAs substrate **201** by a thin film deposition technique like evaporation. Then, part of the grounded conductor layer **202**, which is located just under the region where the line **204** is to be formed, is etched away. To shape the grounded conductor layer **202** into such a pattern, a resist pattern (not shown) may be defined on the grounded

conductor layer **202** and then a portion of the grounded conductor layer **202**, which is not covered with the resist pattern, may be removed by an ion milling technique, for example. In this manner, an opening **205** with a width of about 10μm is provided in the grounded conductor layer **202**. The thickness of the grounded conductor layer **202** is defined within the range from about 0.5μm to about 3μm. The grounded conductor layer **202** is not necessarily made of titanium and gold, but may be made of platinum (Pt) and tungsten silicon nitride (WSiN).

Next, as shown in Figure **5B**, the first strontium titanate layer **203** with a dielectric constant of about 100 is deposited by RF sputtering to be about 1.5 μm thick on the grounded conductor layer **202**.

Thereafter, as shown in Figure **5C**, the gold-plated line **204** is formed on the first strontium titanate layer **203**. In this embodiment, the thickness of the line **204** is 3μm, the width **206** thereof is 15μm, and the centerline of the region where the grounded conductor layer **202** does not exist (i.e., the opening **205**) is substantially aligned with that of the line **204**.

Subsequently, as shown in Figure **5D**, the second strontium titanate layer **207** is deposited over the first strontium titanate layer **203** to cover the line **204**.

Figure **6** illustrates respective angles of phase rotation

for a microstrip line with the structure just described and for the conventional structure shown in Figure **16**. In the example illustrated in Figure **6**, the lengths of these two types of lines are supposed to be equal to each other. Each of these angles of phase rotation represents a phase angle of an associated line on a Smith chart, where the far end of the line is short-circuited. And the angle can be used as an index for estimating a line length required for attaining desired impedance matching. More specifically, the larger the angle of phase rotation of a line, the shorter that portion of the line required for realizing desired impedance matching. As can be seen from Figure **6**, the angle of phase rotation of the line structure according to this embodiment is about 116 degrees larger than that of the conventional structure of the same length. Accordingly, the line length can be shortened according to the present invention compared to the conventional structure. This is because the conventional structure requires a line length, which is longer than that required by the inventive structure by a quantity corresponding to the angle of phase rotation of 116 degrees, for attaining desired impedance matching.

By using such a line structure, the line length of a spiral inductor required for matching the impedance of an active component with a desired load impedance or attaining a desired choke inductance can be shortened, thus reducing the

parasitic resistive components involved with the spiral inductor. As a result, it is possible to provide a semiconductor device operable at radio frequencies and contributing to both downsizing and performance enhancement of mobile communications unit terminals.

The second strontium titanate layer **207**, covering the line **204**, preferably has a dielectric constant higher than 10. This is because the electrical length can be reduced even more drastically by covering the line with a film having a high dielectric constant. Examples of such films with high dielectric constants include a BST film, as well as a strontium titanate film.

Also, the dielectric film provided between the grounded conductor layer **202** and the line **204** may have a multilayer structure including a first dielectric layer and a second dielectric layer formed on the first dielectric layer. In such a case, the dielectric constant of the first dielectric layer may be either higher or lower than that of the second dielectric layer.

EMBODIMENT 3

A third exemplary embodiment of a semiconductor device according to the present invention will be described with reference to Figures **7** through **9**.

Figure **7** illustrates the cross section of a novel line

structure applicable to the semiconductor device of the present invention. As shown in Figure **7**, this line structure includes: a first strontium titanate layer **303** formed on the surface of a GaAs substrate **301**; a grounded conductor layer **302** and a line **305**, which are both made of gold plated to be about 0.7μm thick on the first strontium titanate layer **303**; and a second strontium titanate layer **304** formed to cover the grounded conductor layer **302** and the line **305**. In this specification, the combination of the grounded conductor layer **302** and the line **305** will be called a "coplanar structure". A gap is provided between the line **305** and the grounded conductor layer **302**.

An RF active component, like a MESFET as described in the background section, is actually formed on the GaAs substrate **301**, but is not shown in Figure **7** for the sake of simplicity.

Hereinafter, a method for forming the line structure will be described with reference to Figures **8A** through **8C**.

First, as shown in Figure **8A**, the strontium titanate layer **303** with a dielectric constant of about 100 is deposited by RF sputtering to be about 1.5μm thick on the GaAs substrate **301**.

Next, as shown in Figure **8B**, a conductor film, made up of titanium and gold layers alternately stacked, is deposited to be about 3μm thick on the strontium titanate layer **303** by

a thin film deposition technique like evaporation. The thickness of the conductor film is defined within the range from about 0.5μm to about 6μm, for example. Then, the conductor film is patterned by lithography and etching processes, thereby forming the grounded conductor layer **302** and the line **305** at the same time. In this embodiment, the width **306** of the line **305** is defined at about 15μm, and the width of the space **307** between the line **305** and the grounded conductor layer **302** is also defined at about 15μm. The material of the conductor film is not limited to titanium and gold, but may be plated gold or aluminum (Al). The width of the space **307** is not necessarily 15μm, but may be appropriately selected within the range from about 5μm to about 100μm.

Subsequently, as shown in Figure **8C**, the strontium titanate layer **304** with a dielectric constant of about 100 is deposited by RF sputtering to be about 1.5μm thick and to cover the grounded conductor layer **302** and the line **305**.

Figure **9** illustrates respective angles of phase rotation for a microstrip line with the structure just described and for the conventional structure shown in Figure **16**. In the example illustrated in Figure **9**, the lengths of these two types of lines are supposed to be equal to each other. Each of these angles of phase rotation represents a phase angle of an associated line on a Smith chart, where the far end of the line is short-circuited. And each angle can be used as an

index for estimating a line length required for attaining desired impedance matching. More specifically, the larger the angle of phase rotation of a line, the shorter that portion of the line required for realizing desired impedance matching. As can be seen from Figure **9**, the angle of phase rotation of the line structure according to this embodiment is about 106 degrees larger than that of the conventional structure of the same length. Accordingly, the line length can be shortened according to the present invention compared to the conventional structure.

By using such a line structure, the line length of a spiral inductor required for matching the impedance of an active component with a desired load impedance or attaining a desired choke inductance can be shortened, thus reducing the parasitic resistive components involved with the spiral inductor. As a result, it is possible to provide a semiconductor device operable at radio frequencies and contributing to both downsizing and performance enhancement of mobile communications unit terminals.

The first strontium titanate layer **303**, provided between the grounded conductor layer **302** and the substrate **301** and between the line **305** and the substrate **301**, and the second strontium titanate layer **304**, covering the line **305** and the layer **302**, preferably have a dielectric constant higher than 10. This is because the electrical length can be reduced

even more drastically by covering the line with a dielectric film having a high dielectric constant. Examples of such films with high dielectric constants include a BST film, as well as a strontium titanate film.

Also, the first strontium titanate layer **303**, provided between the grounded conductor layer **302** and the substrate **301** and between the line **305** and the substrate **301**, may have a multilayer structure including a first dielectric layer and a second dielectric layer formed on the first dielectric layer. In such a case, the dielectric constant of the first dielectric layer may be either higher or lower than that of the second dielectric layer.

EMBODIMENT 4

A fourth exemplary embodiment of a semiconductor device according to the present invention will be described with reference to Figure **18**.

Figure **18** illustrates the cross section of a novel line structure applicable to the semiconductor device of the present invention. As shown in Figure **18**, this line structure includes: a grounded conductor layer **702** made up of plural pairs of titanium and gold layers alternately stacked to be about 0.7μm thick on the surface of a GaAs substrate **701**; and a gold-plated line **705** provided over the grounded conductor layer **702** to be spaced apart therefrom. A multilayer struc-

ture, including a silicon nitride film **703** (thickness: about 0.1 μm to about 2.0 μm) and a strontium titanate ($SrTiO_3$) film (thickness: about 0.1 μm to about 2.0 μm) **704**, is formed on the grounded conductor layer **702**. An RF active component, like a MESFET as described in the background section, is actually formed on the GaAs substrate **701**, but is not shown in Figure **18** for the sake of simplicity.

By controlling the thicknesses of the silicon nitride film **703** and strontium titanate ($SrTiO_3$) film **704**, the capacitance formed between the layer **702** and the line **705** can be reduced and the increase in electrical length can be suppressed.

It should be noted that the member(s) **103** and/or **104** of the first embodiment may have such a multilayer structure including a plurality of layers with mutually different dielectric constants.

While the present invention has been described in a preferred embodiment, it will be apparent to those skilled in the art that the disclosed invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

WHAT IS CLAIMED IS:

1. A semiconductor device with a line structure formed on a semiconductor substrate,

wherein the line structure comprises:

a conductor layer formed on the semiconductor substrate;

a dielectric film formed on the conductor layer; and

a conductor line formed on the dielectric film, and

wherein the dielectric film comprises:

a first dielectric portion, at least part of the first dielectric portion being located between the lower surface of the conductor line and the upper surface of the conductor layer; and

second and third dielectric portions laterally arranged to interpose the first dielectric portion therebetween, and

wherein the dielectric constant of the first dielectric portion is different from at least one of the dielectric constants of the second and third dielectric portions.

2. The device of Claim 1, wherein the dielectric constant of the first dielectric portion is lower than those of the second and third dielectric portions.

3. The device of Claim 1 or 2, wherein at least one of the dielectric constants of the second and third dielectric portions is higher than 10.

4. The device of Claim 1 or 2, further comprising another dielectric film covering the conductor line.

5. The device of Claim 1 or 2, further comprising an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

6. A semiconductor device with a line structure formed on a semiconductor substrate,

wherein the line structure comprises:

a conductor layer formed on the semiconductor substrate;

a dielectric film formed on the conductor layer; and

a conductor line formed on the dielectric film, and

wherein the dielectric film includes two or more dielectric layers with mutually different dielectric constants.

7. The device of Claim 6, wherein at least one of the two or more dielectric layers comprises:

a first dielectric portion, at least part of the first dielectric portion being located between the lower surface of the conductor line and the upper surface of the conductor layer; and

second and third dielectric portions laterally arranged to interpose the first dielectric portion therebetween, and

wherein the dielectric constant of the first dielectric portion is different from at least one of the dielectric constants of the second and third dielectric portions.

8. The device of Claim 6, wherein at least one of the two or more dielectric layers has been patterned.

9. A semiconductor device with a line structure formed on a semiconductor substrate,

wherein the line structure comprises:

a conductor layer formed on the semiconductor substrate;

a first dielectric film formed on the conductor layer;

a conductor line formed on the first dielectric film; and

a second dielectric film covering the conductor line.

10. The device of Claim 9, wherein the first dielectric film includes two or more dielectric layers with mutually different dielectric constants.

11. A semiconductor device with a line structure formed on a semiconductor substrate,

wherein the line structure comprises:

a conductor layer formed on the semiconductor substrate;

a dielectric film formed on the conductor layer; and

a conductor line formed on the dielectric film, and

wherein a region of the conductor layer, which is located under the conductor line, has been removed at least partially.

12. The device of Claim 11, wherein the dielectric film includes two or more dielectric layers with mutually different dielectric constants.

13. The device of Claim 11 or 12, further comprising a second dielectric film covering the conductor line.

14. The device of Claim 13, wherein the dielectric constant of the second dielectric film is higher than 10.

15. The device of Claim 11 or 12, further comprising an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

16. A semiconductor device with a line structure formed on a semiconductor substrate,

wherein the line structure comprises:

a coplanar conductor layer formed over the semiconductor substrate; and

a dielectric film formed on the coplanar conductor

layer,

wherein the coplanar conductor layer includes: a grounded conductor layer; and a conductor line spaced apart from the grounded conductor layer, and

wherein the dielectric constant of the dielectric film is higher than 10.

17. The device of Claim 16, wherein a dielectric with a dielectric constant equal to or smaller than 10 exists between the grounded conductor layer and the conductor line.

18. The device of Claim 16 or 17, further comprising an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

19. A semiconductor device with a line structure formed on a semiconductor substrate,

wherein the line structure comprises:

a first dielectric film formed on the semiconductor substrate;

a coplanar conductor layer formed on the first dielectric film; and

a second dielectric film formed on the coplanar conductor layer.

20. The device of Claim 19, wherein the dielectric constant of at least one of the first and second dielectric films is higher than 10.

21. The device of Claim 20, wherein the first dielectric film includes two or more dielectric layers with mutually different dielectric constants.

22. The device of Claim 19, 20 or 21, further comprising an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

ABSTRACT OF THE DISCLOSURE

A semiconductor device according to the present invention includes a line structure formed on a semiconductor substrate. The line structure includes: a conductor layer formed on the semiconductor substrate; a dielectric film formed on the conductor layer; and a conductor line formed on the dielectric film. The dielectric film includes: a first dielectric portion, at least part of the first dielectric portion being located between the lower surface of the conductor line and the upper surface of the conductor layer; and second and third dielectric portions laterally arranged to interpose the first dielectric portion therebetween. The dielectric constant of the first dielectric portion is different from at least one of the dielectric constants of the second and third dielectric portions.

Fig. 1

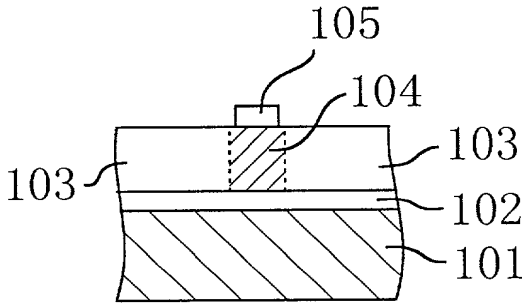


Fig. 2A

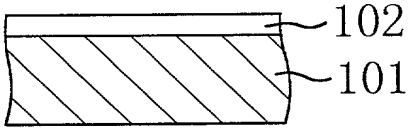


Fig. 2B

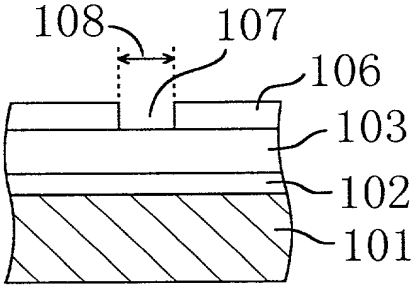


Fig. 2C

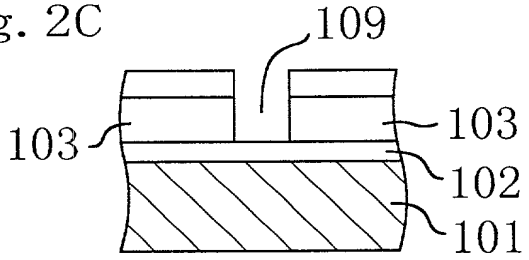


Fig. 2D

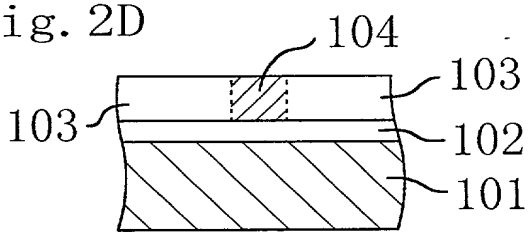


Fig. 2E

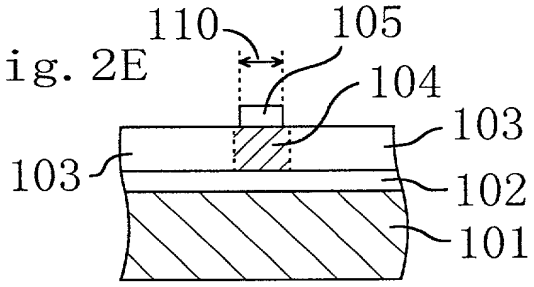


Fig. 2F

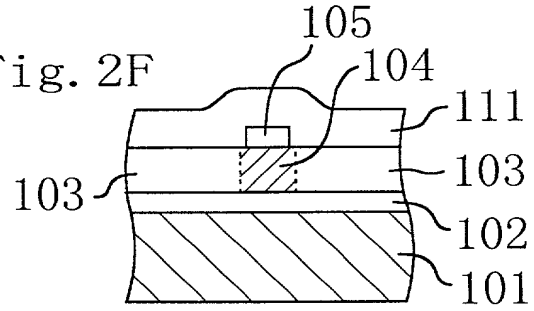
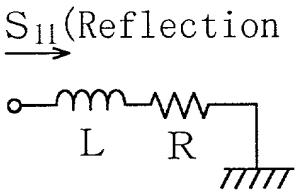


Fig. 3A



L : Equivalent Inductance

R : Equivalent Resistance

Fig. 3B

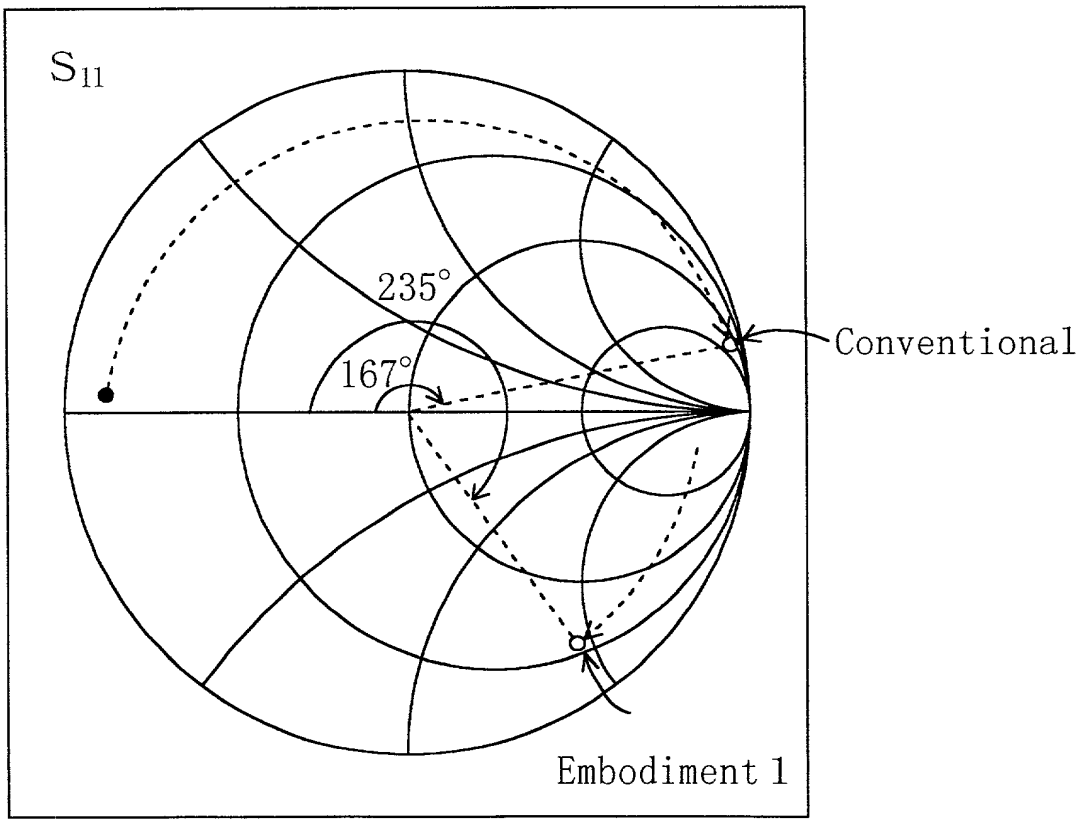


Fig. 4

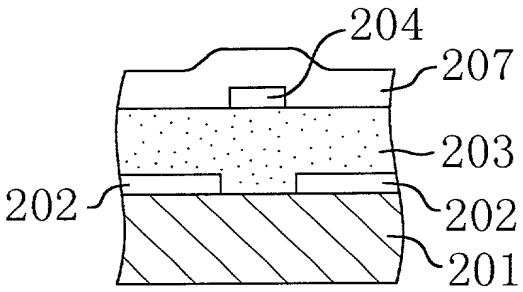


Fig. 5A

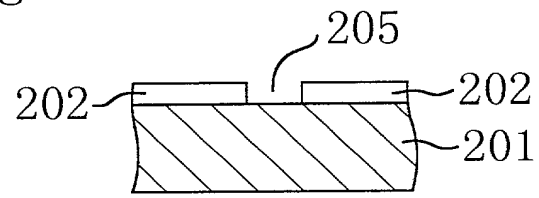


Fig. 5B

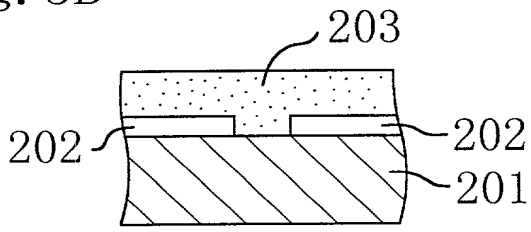


Fig. 5C

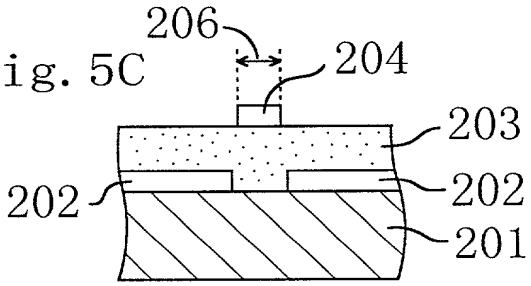


Fig. 5D

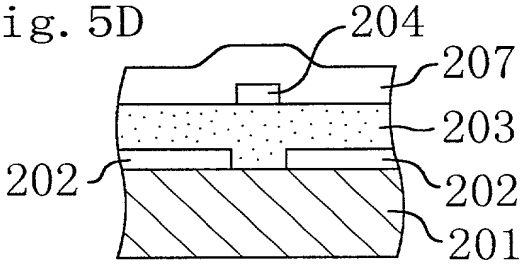


Fig. 6

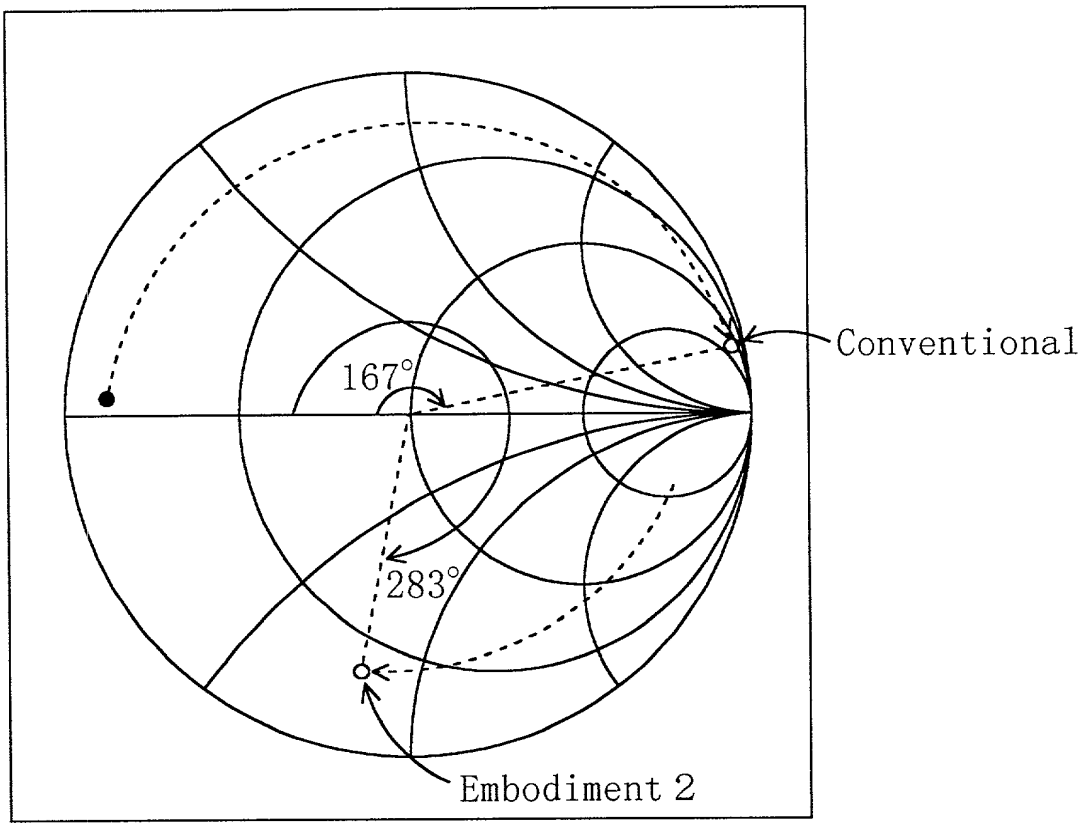


Fig. 7

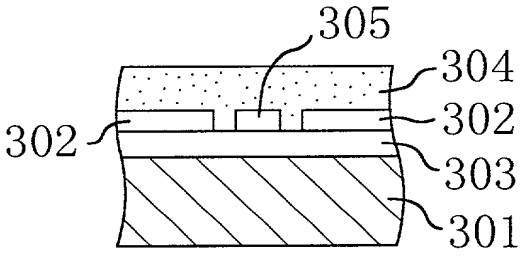


Fig. 8A

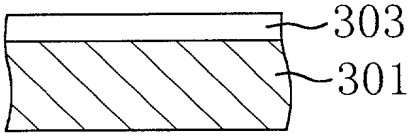


Fig. 8B

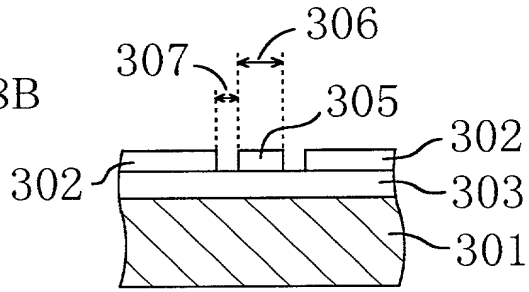


Fig. 8C

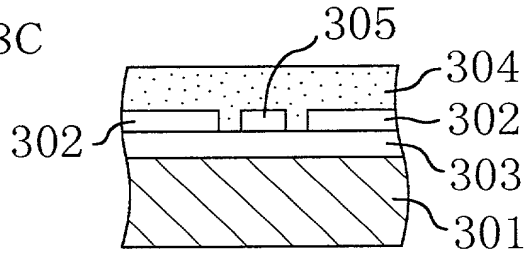


Fig. 9

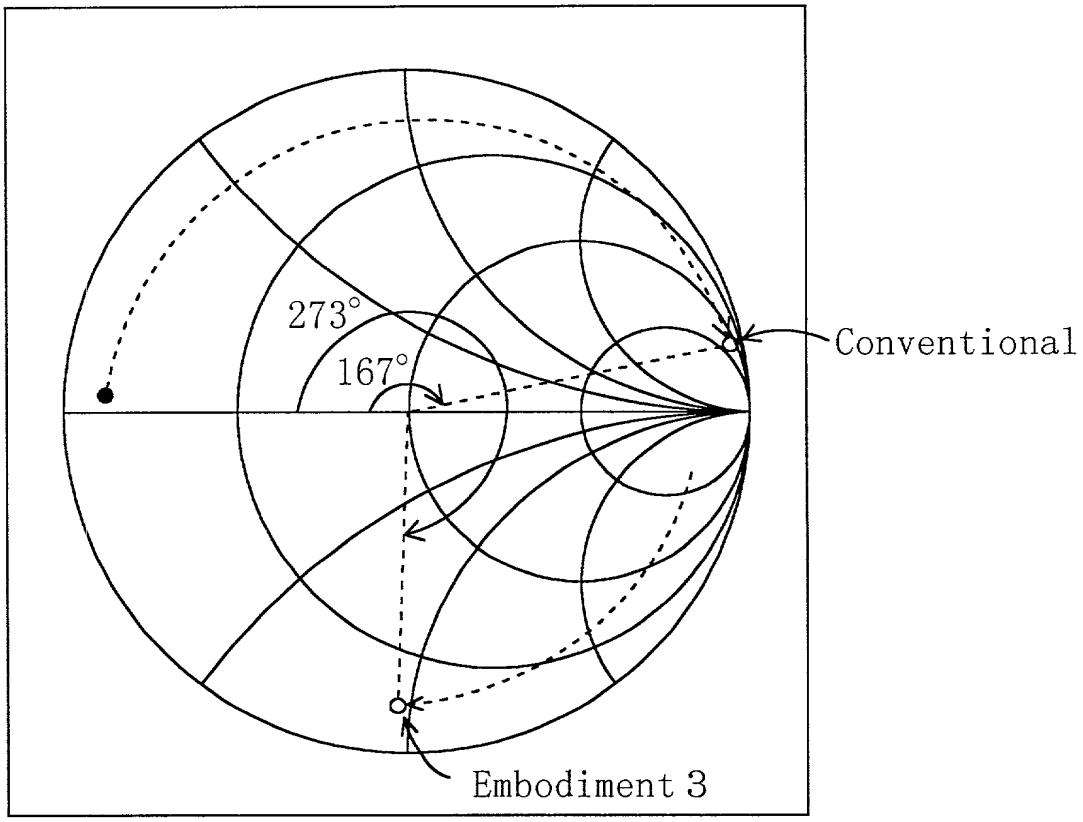


Fig. 10

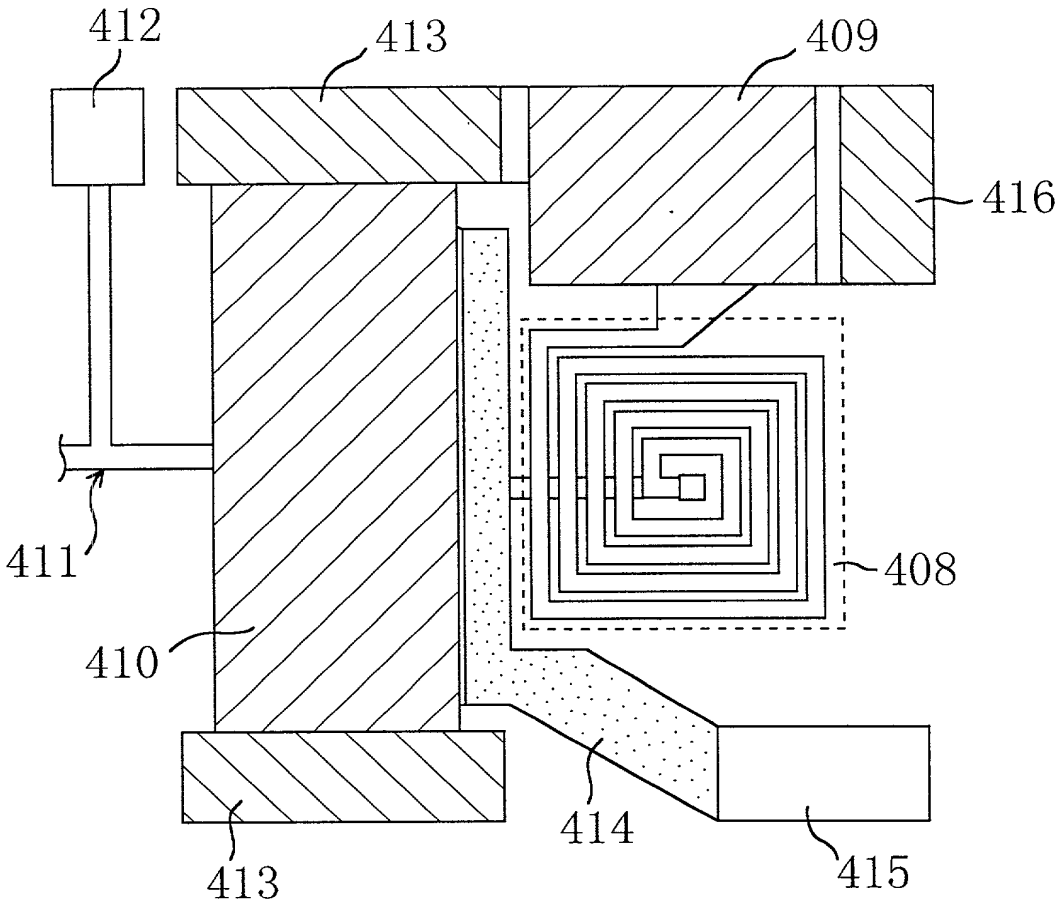

412
413
409
416
411
408
410
414
415
413

Fig. 11

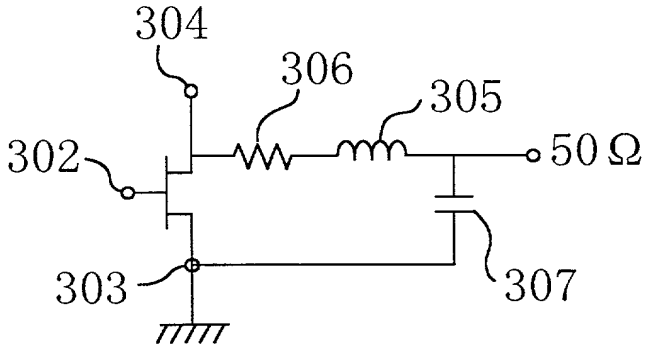

304
306
305
302
50Ω
303
307

Fig. 12

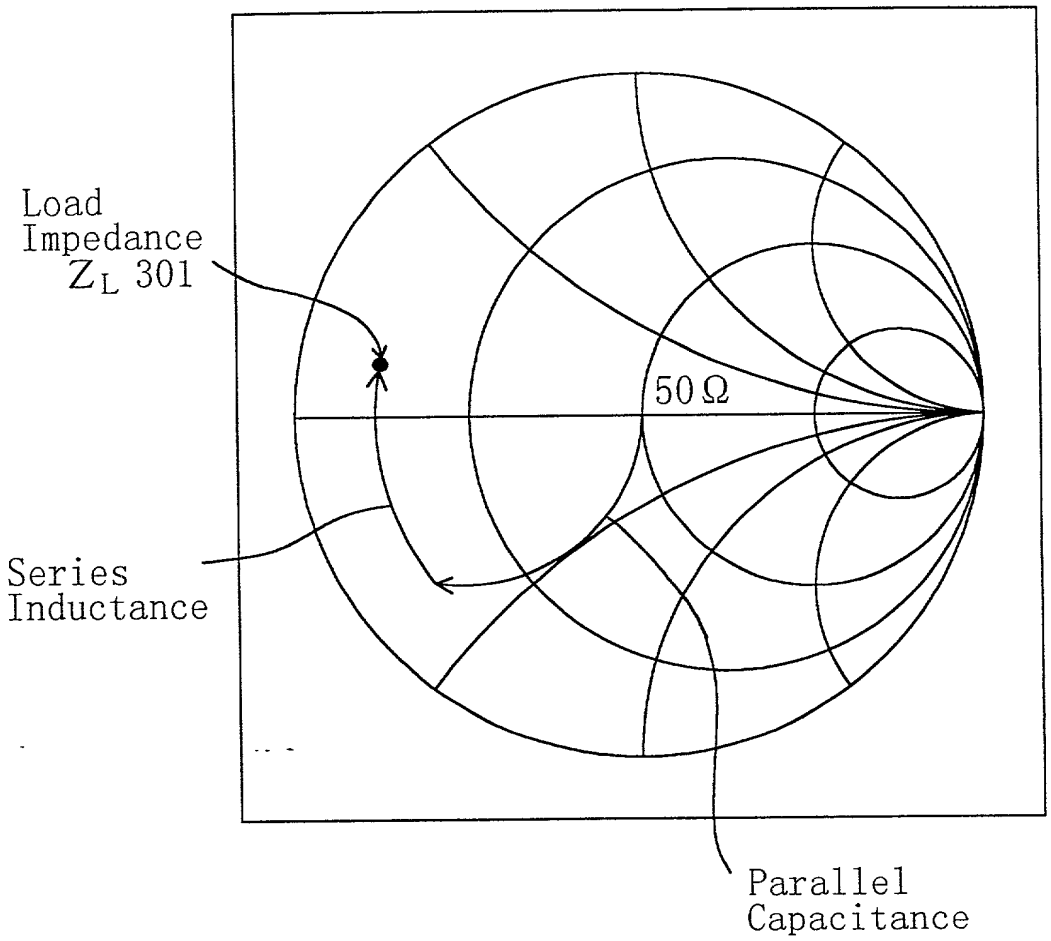

Load
Impedance
Z_L 301
50Ω
Series
Inductance
Parallel
Capacitance

Fig. 13

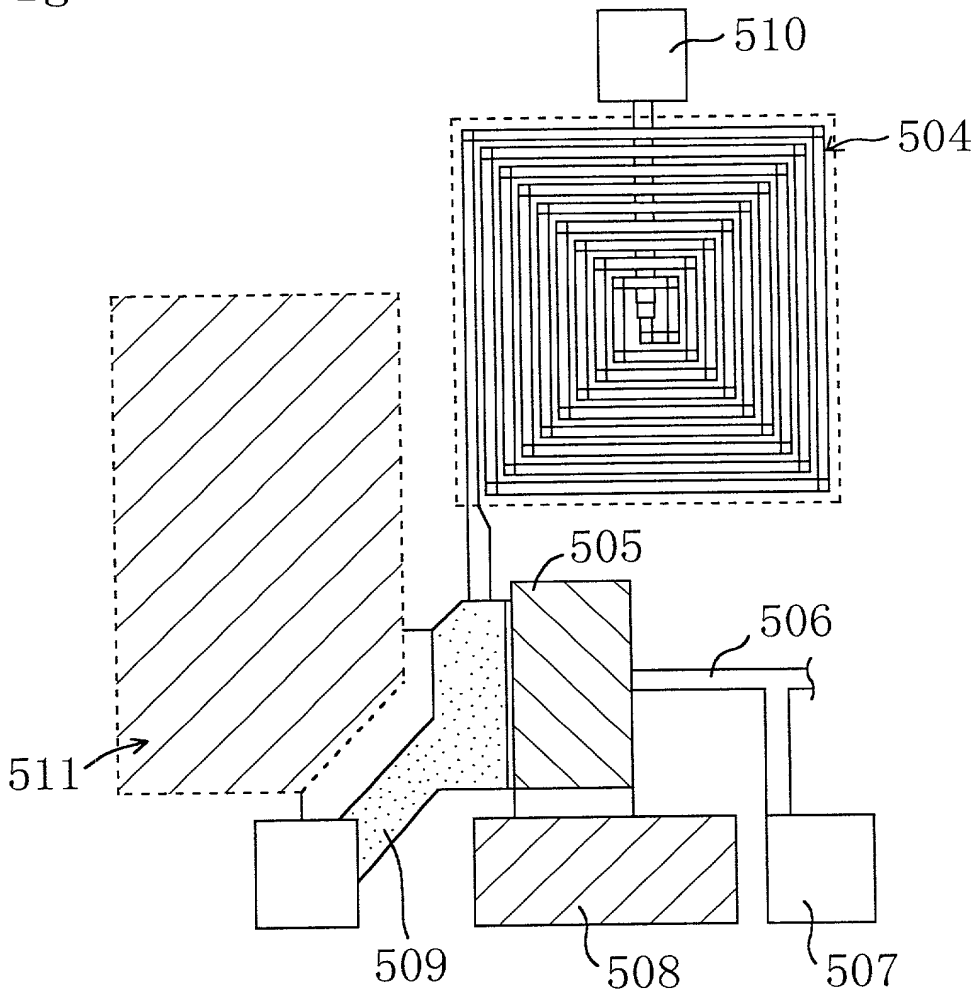

510
504
505
506
511
509
508
507

Fig. 14

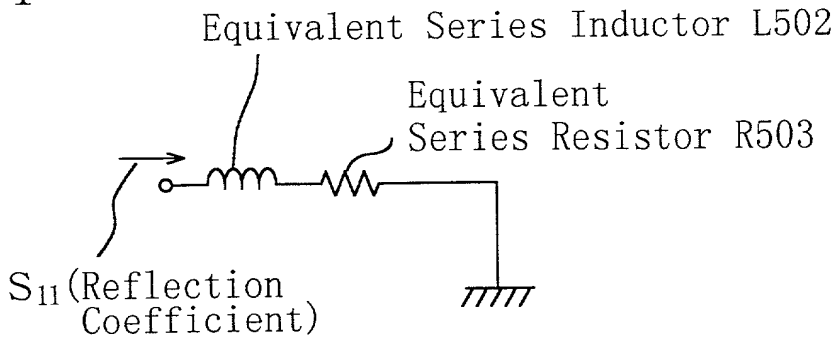

Equivalent Series Inductor L502
Equivalent
Series Resistor R503
S_{11}(Reflection
Coefficient)

Fig. 15

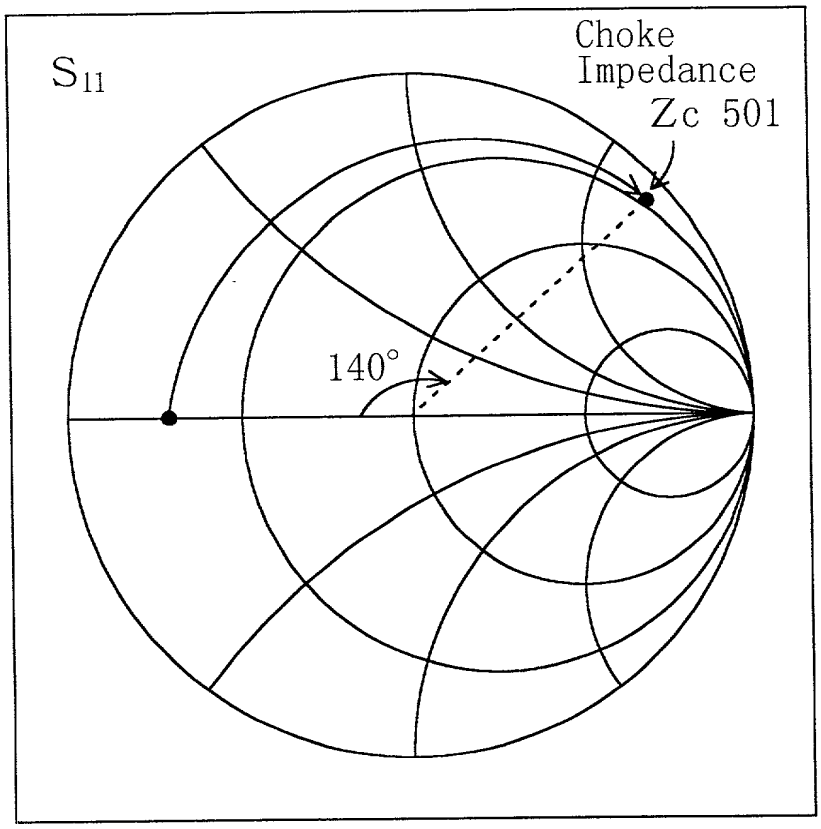


Fig. 16

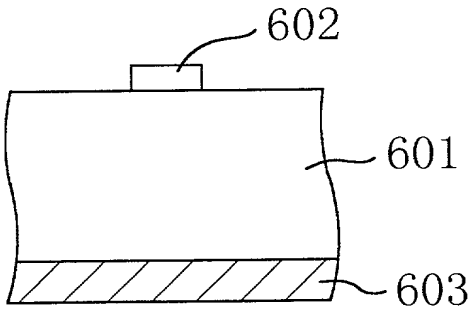


Fig. 17A

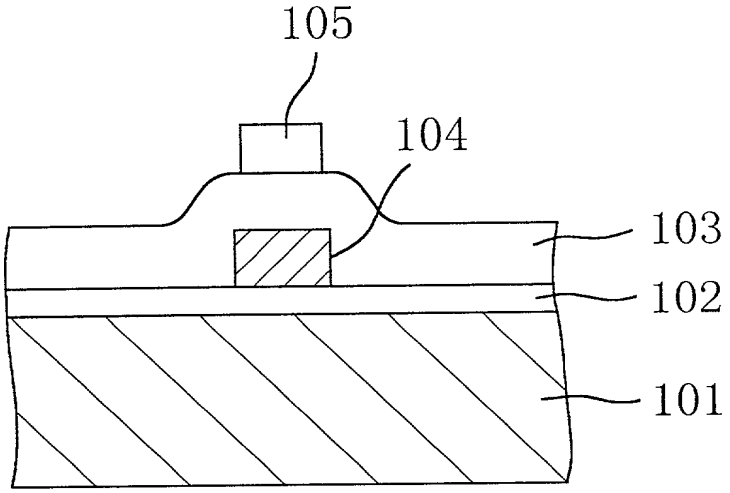


Fig. 17B

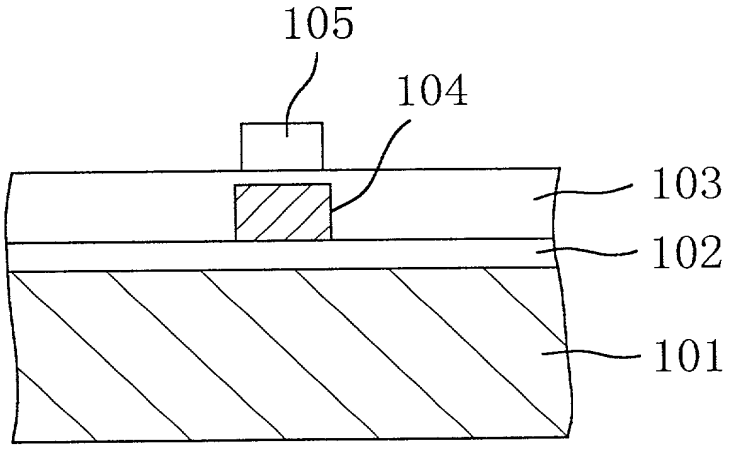


Fig. 18